

external supply voltage to an internal supply voltage lower than said external supply voltage within said chip;

wherein, when said external supply voltage is not higher than a predetermined first voltage, the output voltage of said voltage limiter means increases at a rate which is substantially equal to the increasing rate of said external supply voltage, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said output voltage increases at a rate which is lower than the increasing rate of said external supply voltage, and after said external supply voltage exceeds said second voltage, said internal supply voltage increases at a rate which is higher than the increasing rate thereof when said external supply voltage is between a level exceeding said first voltage and said second voltage.

8. A semiconductor integrated circuit according to claim 7, wherein said internal supply voltage is set so that a stress voltage condition of transistors included in said first circuits is substantially equal to that of transistors included in said second circuits.

9. A semiconductor integrated circuit according to claim 7, wherein the change of said internal supply voltage is made inside said voltage limiter means by detecting a change in said external supply voltage.

10. A semiconductor integrated circuit according to claim 9, wherein said external supply voltage is between a level exceeding said first voltage and ^{G₂} said second voltage when said semiconductor integrated circuit is in a normal operative state, and said external supply voltage exceeds said second voltage when said semiconductor integrated circuit is in an aging state.

⁴ 11. A semiconductor integrated circuit according to claim ³ 10, wherein the ^{third} rate of change of said internal supply voltage when said external supply voltage is between a level exceeding said second voltage and a predetermined third voltage is ^{larger} ^{a fourth} ^{higher} than the rate of change of said internal supply voltage after said external supply voltage exceeds said third voltage.

^{Sub 312} 12. A semiconductor integrated circuit according to claim 11, wherein, when said external supply voltage is between said first voltage and said second voltage, ^{the magnitude of} said internal supply voltage is substantially constant.

^{Sub 6} 13. A semiconductor integrated circuit comprising:
a chip;
load circuits provided on said ^C chip; and
a voltage limiter means provided on said chip for reducing an external supply voltage to an internal supply voltage lower

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than said external supply voltage within said chip and supplying it to said load circuits;

wherein the internal supply voltage is output from said voltage limiter means in response to the operation of said load circuits by controlling a signal for controlling said voltage limiter means and a signal for controlling said load circuits.

14. A semiconductor integrated circuit according to claim 13, wherein said internal supply voltage is set so that a stress voltage condition of transistors constituting said load circuits is substantially equal to that of transistors constituting said voltage limiter means.

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15. A semiconductor integrated circuit according to claim ¹³~~14~~, wherein the change of said internal supply voltage is made inside said ~~voltage limiter~~ *internal power supply* means by detecting a change in said external supply voltage.

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16. A semiconductor integrated circuit according to claim 15, wherein, when said external supply voltage is not higher than a predetermined first voltage, the output voltage of said voltage limiter means increases at a rate which is substantially equal to the increasing rate of said external supply voltage, when said external supply voltage is between a level exceeding said first voltage and a predetermined second voltage, said output voltage increases at a rate which is lower than the increasing rate of

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said external supply voltage, and after said external supply voltage exceeds said second voltage, said internal supply voltage increases at a rate which is higher than the increasing rate thereof when said external supply voltage is between a level exceeding said first voltage and said second voltage.

17. A semiconductor integrated circuit according to claim 16, wherein said external supply voltage is between a level exceeding said first voltage and said second voltage when said semiconductor integrated circuit is in a normal operative state, and said external supply voltage exceeds said second voltage when said semiconductor integrated circuit is in an aging state.

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18. A semiconductor integrated circuit according to claim ⁸ 17, wherein the ^{third} rate of change of said internal supply voltage when said external supply voltage is between a level exceeding said second voltage and a predetermined third voltage is ^{larger} higher than ^{a fourth} the rate of change of said internal supply voltage after said external supply voltage exceeds said third voltage.

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19. A semiconductor integrated circuit according to claim 18, wherein, when said external supply voltage is between said first voltage and said second voltage, ^{the magnitude of} said internal supply voltage is substantially constant.